

AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

Claim 1 (currently amended): A timing controller comprising:

- a first circuit having a first delay time;
- a second circuit having a second delay time; and
- a time difference expander for expanding a time difference between a changeover point of a first signal and a changeover point of a second signal $[[a]] \underline{N}$ times ($[[a]] \underline{N}$ being a value greater than one), to provide an output signal having a given time difference with respect to a control signal, the first signal being passed through said first circuit and said second circuit, and the second signal being passed through said first circuit.

Claim 2 (original): A timing controller as claimed in claim 1, wherein the delay time of said second circuit is substantially equal to the delay time of said first circuit.

Claim 3 (original): A timing controller as claimed in claim 2, wherein said first circuit is an input buffer, and said second circuit is a delay circuit.

Claim 4 (original): A timing controller as claimed in claim 1, wherein the first signal involves the first delay time plus the second delay time with respect to the control signal, the second signal involves the first delay time with respect to the control signal, and the time difference is an interval between a changeover point of the first signal and a one-cycle-behind changeover point of the second signal.

Claim 5 (original): A timing controller as claimed in claim 1, wherein the first signal involves the first delay time plus the second delay time with respect to the control signal, the second signal involves the first delay time with respect to the control signal and a period twice as long as that of the control signal, and the time difference is an interval between a rise of the first signal and a fall of the second signal.

Claim 6 (original): A timing controller as claimed in claim 1, wherein said time difference expander doubles the time difference.

Claim 7 (original): A timing controller as claimed in claim 1, wherein the control signal is a clock signal.

Claim 8 (original): A timing controller as claimed in claim 1, wherein said second circuit comprises a first delay circuit and a second delay circuit, said first delay circuit involving

a fourth delay time that is substantially equal to a third delay time of a signal transmitter for transmitting an output of said time difference expander to a circuit of the next stage, and said second delay circuit having a second delay time that is substantially equal to the first delay time.

Claim 9 (original): A timing controller as claimed in claim 8, wherein said time difference expander expands a time difference between a changeover point of the first signal and a changeover point of the second signal N times (N being an integer equal to or greater than two), to provide an output signal that is inphase with the control signal; the first signal is passed through said first circuit, said first delay circuit, and said second delay circuit; and the second signal is passed through said first circuit.

Claim 10 (original): A timing controller as claimed in claim 1, wherein said timing controller provides an output signal before a rise or fall of the control signal and sustains the output signal for a given period around the rise or fall of the control signal.

Claim 11 (original): A timing controller comprising an internal circuit, and a time difference expander for expanding a time difference between a changeover point of a first signal and a changeover point of a second signal N times (N being an integer equal to or greater than two), to provide a phase-controlled output signal, the first signal being passed through said internal circuit and produced by a cycle of a control signal, and the second signal being passed

through a part of said internal circuit and produced by the next cycle of the control signal.

Claim 12 (original): A timing controller as claimed in claim 11, wherein the control signal is a clock signal.

Claim 13 (original): A timing controller as claimed in claim 11, wherein said timing controller provides an output signal before a rise or fall of the control signal and sustains the output signal for a given period around the rise or fall of the control signal.

Claim 14 (original): A timing controller comprising a first internal circuit, a time difference expander for expanding a time difference between a changeover point of a first signal and a changeover point of a second signal N times (N being an integer equal to or greater than two), to provide a phase-controlled output signal, and a second internal circuit for producing a phase-controlled signal according to an output of said time difference expander, the first signal being passed through said first internal circuit and produced by a cycle of a control signal, the second signal being passed through a part of said first internal circuit and produced by the next cycle of the control signal, a delay time of said second internal circuit being substantially equal to a delay time of a specific part of said first internal circuit.

Claim 15 (original): A timing controller as claimed in claim 14, wherein the control

signal is a clock signal.

Claim 16 (original): A timing controller as claimed in claim 14, wherein said timing controller provides an output signal before a rise or fall of the control signal and sustains the output signal for a given period around the rise or fall of the control signal.

Claim 17 (withdrawn): An electric circuit comprising:
a first clock buffer circuit receiving an external clock signal;
a first clock delivery circuit; and
a first clock timing control circuit, being supplied with an output of said first clock buffer circuit and an output of said first clock delivery circuit, for generating a preceding internal clock before the output of said first clock buffer circuit being output.

Claim 18 (withdrawn): An electric circuit comprising:
a first clock buffer circuit receiving an external clock signal;
a first clock delivery circuit;
a first delay circuit for duplicating delay time characteristics of said first clock buffer circuit;
and
a first clock timing control circuit, being supplied with an output of said first clock buffer circuit and an output of said first delay circuit, for generating a preceding internal clock before the

output of said first clock buffer circuit being output.

Claim 19 (withdrawn): An electric circuit as claimed in claim 18, wherein said first delay circuit duplicates delay time characteristics of said first clock buffer circuit and said first clock delivery circuit.

Claim 20 (withdrawn): An electric circuit as claimed in claim 18, wherein said electric circuit further comprises a first optional circuit, and said first delay circuit duplicates delay time characteristics of said first clock buffer circuit, said first clock delivery circuit, and said first optional circuit.

Claim 21 (withdrawn): An electric circuit as claimed in claim 20, wherein said electric circuit further comprises a first clock frequency control circuit for receiving an output of said clock buffer circuit, and an output of said first clock frequency control circuit is also supplied to said first clock timing control circuit.

Claim 22 (withdrawn): An electric circuit as claimed in claim 20, wherein said first clock timing control circuit stores capability information into a memory, and the capability information relates to the input from the output of said first clock buffer circuit and the output of said first delay circuit.

Claim 23 (withdrawn): An electric circuit comprising:

a first clock buffer circuit receiving an external clock signal;

a first clock delivery circuit; and

a first clock timing control circuit, being supplied with an output of said first clock buffer circuit and an output of said first clock delivery circuit, for generating an output coincident with said external clock signal.

Claim 24 (withdrawn): An electric circuit comprising:

a first clock buffer circuit receiving an external clock signal;

a first clock delivery circuit;

a first delay circuit for duplicating delay time characteristics of said first clock buffer circuit; and a first clock timing control circuit, being supplied with an output of said first clock buffer circuit and an output of said first delay circuit, for generating an output coincident with said external clock signal.

Claim 25 (withdrawn): An electric circuit as claimed in claim 24, wherein said first delay circuit duplicates delay time characteristics of said first clock buffer circuit and said first clock delivery circuit.

Claim 26 (withdrawn): An electric circuit as claimed in claim 24, wherein said electric

circuit further comprises a first optional circuit, and said first delay circuit duplicates a delay time characteristics of said first clock buffer circuit, said first clock delivery circuit, and said first optional circuit.

Claim 27 (withdrawn): An electric circuit as claimed in claim 26, wherein said electric circuit further comprises a first clock frequency control circuit for receiving an output of said clock buffer circuit, an output of said first clock frequency control circuit is also supplied to said first clock timing control circuit, and said first clock timing control circuit generates an output coincident with a part of said external clock signal.

Claim 28 (withdrawn): An electric circuit as claimed in claim 26, wherein said first clock timing control circuit stores capability information into a memory, the capability information relates to the input from the output of said first clock buffer circuit and the output of said first delay circuit, and said first clock timing control circuit generates an output coincident with a part of said external clock signal.

Claim 29 (new): A timing controller comprising:

- a. first delay circuit receiving a first clock signal and outputting a second clock signal;
- a variable delay circuit, receiving the first and second clock signals and delaying the second clock signal, and having a delay time determined by expanding a time difference from a first timing

of inputting the second, clock signal to a second timing of changing the first clock signal N times (N being an integer equal to or greater than two); and

a second delay circuit connected to said first delay circuit and said variable delay circuit in series, and thereby said timing controller generates a control clock signal having a given time difference with respect to the first clock signal.

Claim 30 (new): A timing controller as claimed in claim 29, wherein said N times is two times.

Claim 31 (new): A timing controller as claimed in claim 29, wherein the delay time of said first delay circuit is substantially equal to the delay time of said second delay circuit.

Claim 32 (new): A timing controller as claimed in claim 29, wherein a change timing of the control clock signal is consistent with a change timing of the first clock signal.

Claim 33 (new): A timing controller as claimed in claim 29, wherein said first delay circuit has a delay time corresponding to total delay times of an input buffer, a wiring, and an output buffer.

Claim 34 (new): A timing controller as claimed in claim 29, wherein the delay time of said second delay circuit is shorter than that of said first delay circuit.

Claim 35 (new): A timing controller as claimed in claim 29, wherein the delay time of said second delay circuit is shorter by the delay time of an output buffer than the delay time of said first delay circuit.

Claim 36 (new): An electronic circuit having a timing controller and an output buffer, said output buffer receiving a control clock signal and outputting signal in response to the control clock signal, said timing controller comprising:

a first delay circuit receiving a first clock signal and outputting a second clock signal;

a variable delay circuit, receiving the first and second clock signals and delaying the second clock signal, and having a delay time determined by expanding a time difference from a first timing of inputting the second clock signal to a second timing of changing the first clock signal N times (N being an integer equal to or greater than two); and

a second delay circuit connected to said first delay circuit and said variable delay circuit in series, and thereby said timing controller generates said control clock, signal having a given time difference with respect to the first clock signal.